AMENDMENTS TO THE DRAWINGS

The Examiner has objected to the drawings as having certain deficiencies. To address these deficiencies, the attached sheets of drawings include changes to Figures 2, 3 and 4. These sheets replace the previously submitted sheets of Figures 2, 3 and 4.

In Figure 2, 28A-28C are amended to include the wording "ITERATIVE PROCESS", 34A-34C are amended to change GATES to "NETLIST" and 36 is amended to change GATES to "NETLIST". In addition, Figure 2 is amended to provide the TOP-LEVEL RTL to 30A and 30C as shown in the originally filed drawings.

In Figure 3, 48 is amended to be "GATE LEVEL DESIGN" as described on page 2, lines 1-3 of the originally filed specification.

In Figure 4, each of 64A-64C is respectively amended to be "SYNTHESIZE GATE LEVEL DESIGN OF SUB-MODULE (A-C)", each of 68A-68C is respectively amended to be "GENERATE SUB-MODULE (A-C) NETLIST". 70 is amended to be "INTEGRATE SUB-MODULES NETLISTS TO FORM INTEGRATED TOP-LEVEL NETLIST", and 71 is amended to be "PERFORM STATIC TIMING ANALYSIS FOR INTEGRATED TOP-LEVEL DESIGN NETLIST".

With respect to changing the output of decision block #58 of Figure 3 to be shown as returning the input arrow to block #50, this would be inappropriate as the output is designated as "To Any Previous Process Depending on Analysis" and is consistent with the description at lines 28-31 of page 4 that "If the requirements are not met, the process returns back to one of the previous process steps, depending on which requirements are not met. The process is iterated to optimize or re-synthesize to meet the timing requirements for that sub-module." Clearly, there

may be a previous process step prior to the verifications which are included in optimizing or re-synthesizing to meet the timing requires for that sub-module.

REMARKS/ARGUMENTS

In response to the Office Action dated December 22, 2004, claims 2, 5-7, 9, 10 and 12-17 are amended, and claims 3 and 11 are cancelled. Claims 2, 5-10 and 12-17 are now active in this application. No new matter has been added.

OBJECTION TO THE SPECIFICATION

The Examiner objects to the description at page 4, lines 21-23 of the specification. By this response, the paragraph that includes these lines is amended to describe that "The synthesis/optimization process uses these inputs to generate the gate level design as depicted in blocks 46 and 48. Based upon the gate level design, verification is performed and is represented by block 50. The verifications include a static timing analysis 52, dynamic simulation of the circuitry 54, and other formal verifications typically used in RTL-based design. When the requirements are met, as depicted by decision block 58, the synthesis of gate level design of the sub-module is complete and ready for production of a netlist for that sub-module. Referring back to Figure 2, the sub-module netlist for that sub-module may then be integrated with the other sub-module netlists to form a top-level netlist for the top-level design. If the requirements are not met, the process returns back to one of the previous process steps, depending on which requirements are not met. The process is iterated to optimize or re-synthesize to meet the timing requirements for that sub-module."

This description, along with the change to Figure 3 to describe block 48 as "LOGIC GATE DESIGN" is believed to accurately reflect the invention described. It should be remembered also that a netlist generated for a sub-module is a list of components and connections for the sub-module.

OBJECTION TO THE CLAIMS

Claims 5, 10 and 13 are objected to for minor informalities. With regard to lack of sufficient antecedent support for "the individual sub-blocks" in claims 5 and 13, the claims are amended for consistency with previously reciting "each sub-module" in claims 2, 5 and 10. Therefore, subsequent recitations of "the individual sub-blocks/modules" are changed to recite "said each sub-module".

REJECTION OF CLAIMS UNDER 35 U.S.C. § 112, FIRST PARAGRAPH

Claims 2, 3 an 5-17 are rejected under 35 U.S.C. §112, first paragraph, for failing to comply with enablement requirement. The Examiner maintains that "generating gate-level netlists for the gate-level designs of each of the sub-modules" is not enabled by the present specification. The Examiner appears to repeat this rejection on page 5 of the Official Action.

By this response, the specification is amended to clarify the present invention and the claims are amended to be more clearly directed to the present invention.

The conventional approach to synthesis of an RTL based design of a top-level system is shown in the dashed lines portion at the top of Figure 2 and performs top-level synthesis (of the gate level design) of the top-level system based on specified top-level timing requirements and specified top-level RTL to generate a top-level netlist (which is defined in the specification as a list of components and connections).

In contrast, the present invention as now recited in amended independent claim 2, for example, first there is determined a plurality of sub-modules of a top level system and then individual time budgets for each sub-module based on timing requirements of the top-level system are determined. Next, a gate level design is synthesized for each sub-module based on

the determined time budgets for each sub-module and then the gate level design is tested for conformance with design requirements of the sub-module. If the gate level design conforms, a netlist is generated for the sub-module. After a netlist is generated for each sub-module, the netlists are integrated to form an integrated top level design netlist. The integrated top-level design netlist is then tested for conformance with top-level design requirements and a top-level netlist is generated when the integrated top-level design netlist conforms to the top-level design requirements.

Thus, the conventional approach to synthesis of an RTL based design of a top-level system using logic gate library techniques is concerned with synthesizing gate level design of the top-level system all at once to provide a netlist of the top-level system while the present invention breaks the top-level system into sub-modules and then performs gate level design for the sub-modules to provide a netlist for each sub-module which are then integrated to (ultimately) provide the netlist of the top-level system; i.e., the netlist of the top-level system is derived by integrating the netlist of the individual sub-modules. As noted, the conventional approach to synthesis of an RTL based design of a top-level system using logic gate library techniques is known to a person of ordinary skill in the art. Consequently, the present specification would enable such person of ordinary skill to make and use the invention since synthesizing the gate level design of the sub-modules would use the same techniques used in synthesizing the gate level design of the overall top-level system, but they would be performed at the sub-module level to provide a netlist for each sub-module which are then integrated.

In the present specification, netlist is clearly described as a list of components and connections for the sub-modules. Since the present application describes using logic gate library technology, it is clear also that the components for the netlist would be logic gates from the logic

gate library together with their connections in forming the gate level design of the sub-module. In this technology, it is recognized that it is possible to use different logic gates from the logic gate library in the synthesis of the gate level design of a sub-module. However, while a certain group of interconnected logic gates may make up a gate level design of a sub-module and perform the required functions of the sub-module, such certain group of interconnected logic gates may not meet the design requirements for the sub-module. It is only after a gate level design (a particular group of interconnected logic gates) of a sub-module is determined to meet the design requirements is a netlist for the sub-module provided.

Applicants stress that a patent specification is directed to one having ordinary skill in the art. ***In re Howarth***, 654 F.2d 103, 210 USPQ 689 (CCPA 1981). Accordingly, conventional knowledge is read into this disclosure, relieving Applicants of the burden of disclosing in painstaking detail that which is already known, thereby burdening the Patent and Trademark Office with cumbersome specifications. ***Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.***, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984); ***In re Howarth, supra***. Moreover, and quite significantly, it has been repeatedly held that the scope of enablement varies inversely with the degree of predictability in the art, i.e., enablement is a function of the complexity of the involved subject matter. ***Northern Telecom, Inc. v. Datapoint Corp.***, 908 F.2d 931, 15 USPQ2d 1321 (Fed. Cir. 1990); ***U.S. v. Telectronics Inc., supra***; ***In re Fisher***, 427 F.2d 833, 166 USPQ 18 (CCPA 1970).

As noted above, the subject matter to which the claimed invention is directed is concerned with a modification of the well known process of synthesis of register transfer level (RTL) based design using logic gate library technology. Given that it is known in the art how to synthesize register transfer level (RTL) based design of a top-level design using logic gate library technology, an artisan, using the present disclosure describing applying such technology to the plurality of sub-

modules that make-up the top level design and then integrating the resulting sub-module designs to provide the top-level design, would be able to make and use the invention recited in claims 2, 5-10 and 12-17, as amended.

It is, therefore, Applicants' position that the present specification complies the first paragraph of 35 U.S.C. § 112. Accordingly, withdrawal of the rejection of claims 2, 5-10 and 12-17, as amended, under 35 U.S.C. § 112, first paragraph, is respectfully solicited.

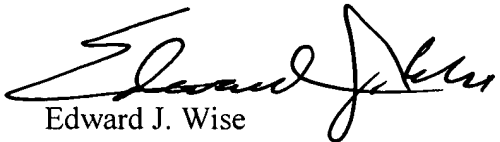
CONCLUSION

Accordingly, it is urged that the application, as now amended, is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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